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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/852,818	05/09/2001	Brian Sander	03942-237	5477

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EXAMINER	
GOSHTASBI, JAMSHID	

ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 10/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/852,818	SANDER, BRIAN	
	Examiner	Art Unit	
	Jamshid Goshtasbi-G.	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/16/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9 are pending in the application.

Drawings

2. Figures 1-3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to under 37 CFR 1.83(a) because they fail to show the clocking of flip flop 401a in logic section 401 and flip flips 405a of logic sections 5.1-5.8 in Fig. 4 by the unknown clock signal Fx as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended.

The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claim 4 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim 4 is improperly dependent on itself, while the recited limitation seems intending to further limit the subject matter of Claim 3.

Claim Rejections – 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US 6326826 B1) in view of Dent (US 5084669).

As to **Claim 1**, Lee et al. discloses a delayed-locked loop including a frequency detection logic and a phase detector comprising forming a sequence of multiple delayed versions of the derived clock signal, each delayed version following a first delayed version in the sequence being delayed more than a previous delayed version in the sequence (a plurality of delay elements adapted to incrementally delaying the input reference clock to generate a set of multiphase clocks; col. 2, lines 1-3), sampling each delayed version of the of the clock time with the known clock signal to produce first intermediate values (frequency detector logic adapted to counting the number of rising edges occurring on the set of multiphase clocks in one period of the input reference clock; col. 2, lines 3-5 and lines 52-55) and performing transition detection using the first intermediate values to produce second intermediate values (frequency detection logic comprises frequency detection cells, where each cell receives a delayed clock CK[N] as a trigger pulse and moves the output (EDGE[N]) from 0 to 1 on the rising edge of CK[N]; col. 3, lines 6-19; i.e., a transition detector), and combining second intermediate values to produce sample values (the decision logic 23 counts the number of 1's in EDGE[1:7] within one period of the input reference clock and may be implemented using Boolean logic, including a

counter; col. 3, lines 19-29). Lee et al., however, fails to teach either forming from the unknown clock signal a derived clock signal or sampling the delayed versions of the derived clock signal with the known clock signal; however, Dent, in describing methods for producing a value representing the instantaneous frequency of a signal (col. 2, lines 26-29), teaches directly generating (determining at specified sampling times; col. 3, lines47-48) values that correctly represent (as a digital code; col. 3, line 49) the phase angle of a pulse train (clock signal) relative to a reference (known) clock signal or pulse train, which are suitable for numerical differentiation or other processing to generate (at specified times interval; col. 3, line21-22) digital representations of instantaneous frequency (col. 3, lines 4-11). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Dent into the method of Lee et al. for producing the claimed invention because sampling delayed versions (Lee et al.) of a derived unknown clock (which may be derived from a communications signal and used as input to the delay chain 10 of Lee et al.) with a known clock signal (Dent; used for sampling the delayed clocks CK[1:7] in the frequency detection logic of Lee et al.) to count the number of rising edges of the delayed versions of the derived unknown clock during one period of the reference (known) clock for consequently determining the frequency of the unknown clock.

Claim 2 inherits all the limitations of Claim 1; further, Lee et al. discloses counting (summing) the number of rising edges (the second intermediate values) of the delayed versions of the clock signal (col. 2, lines 52-55).

Claim 3 inherits all the limitations of Claim 2; further, Lee et al. discloses a decision logic mapping the count (sum) of the rising edges of the delayed clock signals (second intermediate values) to a smaller number of signals (values) indicating a frequency lock or the direction in which frequency needs to be adjusted (col. 3, lines 19-29).

Claim 4 inherits all the limitations of Claim 3 (see the improper dependency of Claim 4, objected to above); further, Lee et al. discloses the decision logic generating (mapping) the frequency lock and direction signals (a smaller number of values) by comparing the count (sum) with a predetermined number (col. 2, lines 7-8) of rising edges (transitions) of the delayed clock signals (according to the anticipated frequency range of the unknown) in one period of the known sampling clock (col. 3, lines 19-23).

As to **Claim 5**, the claimed circuit for sampling an unknown clock signal using a known clock signal recites features that correspond with subject matter mentioned above in the rejection of Claim 1 and are applicable hereto.

Claim 6 inherits all the limitations of Claim 5; further, the claimed apparatus including features that correspond with subject matter mentioned above in the rejection of claims 2 and 3 and are applicable hereto.

Claim 7 inherits all the limitations of Claim 6; further, the claimed apparatus including features that correspond with subject matter mentioned above in the rejection of claims 2, 3, and 4 and are applicable hereto.

As to **Claim 8**, the claimed method for forming (generating) a number stream (a series of binary numbers) representing frequency or phase of an

unknown clock signal using a known clock signal recites features that correspond with subject matter mentioned above in the rejection of claims 1-7 and are applicable hereto; further, Lee et al. discloses applying to the digital circuit a predetermined (alias) value indicating an expected number of rising edges in one period of the known clock signal (frequency range of the unknown clack signal) and forming a number stream (series of binary numbers generated by the counter) and frequency lock and direction numbers in accordance with the alias value (col. 2, lines 7-8; col. 3, lines 19-23).

7. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US 6326826 B1) in view of Dent (US 5084669) as applied to claims 1-8 above, and further in view of Mac Williams et al. (US 5488639).

As to **Claim 9**, the claimed digital circuit for forming (generating) a number stream (a series of binary numbers) representing frequency or phase of an unknown clock signal using a known clock signal recites features that correspond with subject matter mentioned above in the rejection of claims 1-8 and are applicable hereto; further, Williams et al. teaches using flip flops to produce incrementally delayed copies of a clock signal (figures 3 and 5) and to perform sampling (Fig. 4) of an input signal. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Williams et al. into the method of Lee et al. (in view of Dent) for producing the claimed invention because using a chain of flip flops, alternatively, produces incrementally delayed copies of the unknown clock signal, each

delayed clock signal coupled to frequency detection units (combined with more flip flops of FD cells) for sampling and rising edge detection.

Conclusions

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Behrin [US 5761254] and Ampe et al. [US 5272391] provide circuits for sampling an input data signal with incrementally delayed copies of clock signal and teach transition detection. Sander [US 6219394 B1] teaches the use of two chains of flip flops sampling an unknown clock signal with a known clock signal.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jamshid Goshtasbi-G. whose telephone number is (571) 272-3012. The examiner can normally be reached on M-F 8:00/4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through

Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jamshid Goshtasbi-G.
Examiner
Art Unit 2637

KHAI TRAN
PRIMARY EXAMINER